

CALL FOR PAPERS

Second International Workshop on

New Frontiers in High-performance and Hardware-aware Computing (HipHaC'11)

to be held in conjunction with the
17th IEEE International Symposium on High-Performance Computer Architecture
(HPCA-17)

February 13, 2011

San Antonio, Texas, USA

Workshop Organizers:

Rainer Buchty
Eberhard Karls University Tübingen, Germany
Jan-Philipp Weiß
Karlsruhe Institute of Technology, Germany

Steering Committee:

Vincent Heuveline
Karlsruhe Institute of Technology, Germany
Wolfgang Karl
Karlsruhe Institute of Technology, Germany

Program Committee:

David Bader
Georgia Tech, Atlanta, USA
Michael Bader
Univ. Stuttgart, Germany
Mladen Berekovic
Univ. Braunschweig, Germany
Alan Berenbaum
SMSC, USA
Martin Bogdan
Univ. Leipzig, Germany
Dominik Göttsche
TU Dortmund, Germany
Georg Hager
Univ. Erlangen, Germany
Vincent Heuveline
Karlsruhe Institute of Technology, Germany
Eric d'Hollander
Ghent University, Belgium
Michael Hübner
Karlsruhe Institute of Technology, Germany
Ben Juurlink
TU Berlin, Germany
Wolfgang Karl
Karlsruhe Institute of Technology, Germany
Rainer Keller
HLRS, Stuttgart, Germany
Hiroaki Kobayashi
Tohoku University, Japan
Harald Köstler
Univ. Erlangen, Germany
Dieter an Mey
RWTH Aachen, Germany
Andy Nisbet
Manchester Metropolitan University, UK
Christian Perez
INRIA, France
Franz-Josef Pfreundt
ITWM Kaiserslautern, Germany
Wolfgang Rosenstiel
Eberhard Karls University Tübingen, Germany
Olaf Schenk
Basel University, Switzerland
Martin Schulz
LLNL, USA
Mascha Sosonkina
Ames Lab, USA
Thomas Steinke
Zuse-Institut Berlin, Germany
Josef Weidendorfer
TU Munich, Germany
Felix Wolf
GRS-SIM Aachen/Jülich, Germany

Important Dates:

Paper Submission Deadline:
November 28, 2010
December 3, 2010
Notification of Acceptance:
December 19, 2010
Camera-Ready papers:
January 14, 2011
Workshop:
February 13, 2011

Contact:

Rainer Buchty
Eberhard Karls University Tübingen, Germany
buchty@informatik.uni-tuebingen.de

Jan-Philipp Weiß
Karlsruhe Institute of Technology, Germany
jan-philipp.weiss@kit.edu

Links:

Workshop Website
<http://www.hiphac.org/>

Conference Website
<http://www.hpcacnf.org/hpca17/>

Workshop theme: Heterogeneity and reconfigurability in computer systems is growing. Multi- and manycore-based systems are complemented by coprocessors, accelerators and reconfigurable units providing huge computational power. However, applications of scientific interest (e.g. in high-performance computing and numerical simulation) are not yet ready to exploit the available high computing potential. Different programming models, non-adjusted interfaces, and bandwidth bottlenecks complicate holistic programming approaches for heterogeneous architectures. In modern microprocessors, hierarchical memory layouts and complex logics obscure predictability of memory transfers or performance estimations.

For efficient implementations and optimal results, underlying algorithms and mathematical solution methods have to be adapted carefully to architectural constraints like fine-grained parallelism and memory or bandwidth limitations that require additional communication and synchronization. Currently, a comprehensive knowledge of underlying hardware is therefore mandatory for application programmers. Hence, there is strong need for virtualization concepts that free programmers from hardware details, maintaining best performance and enable deployment in heterogeneous and reconfigurable environments.

Possible solutions may consist of supporting libraries, software layers, and tools that automatically care for adaptations of program parameters like block sizes or communication patterns. Autotuning concepts are a possible approach for finding non-obvious optimal choices of such parameters.

This workshop aims at combining new aspects of parallel, heterogeneous, and reconfigurable microprocessor technologies with concepts of high-performance computing and, particularly, numerical solution methods. Compute- and memory-intensive applications can only benefit from the full hardware potential if all features on all levels are taken into account in a holistic approach.

Topics of interest for workshop submissions include (but are not limited to):

- Emerging hardware architectures (multi-/manycores, GPUs, FPGAs, ...)
- High-performance heterogeneous, adaptive, and reconfigurable computing
- Parallelization strategies in hybrid and hierarchical setups
- Hardware-aware computing and code optimization strategies
- Virtualization and software layers for heterogeneous and reconfigurable platforms freeing programmers from dedicated hardware knowledge
- Architecture- and memory-aware approaches for parallel numerical applications, implementation, and algorithm design
- Programming models, compiler techniques, and code-optimization strategies for parallel systems
- Autotuning concepts and run-time adaptivity
- Practice and experience of multi-/manycore programming and application aspects
- Performance evaluation of scientific applications on emerging hardware
- Tools for design, programming, and optimization

Submission guidelines: You are invited to submit papers not exceeding 8 double-column IEEE formatted pages (including up to 6 keywords and an abstract of no more than 350 words), describing original, unpublished recent work related to the workshop theme. Submission must be in PDF format and performed via EasyChair. Please follow the link on the workshop website or submit directly at <http://www.easychair.org/conferences/?conf=hiphac11>. If you wish a blind review to be performed, do not include the author's names and affiliation in the paper.

Papers will be published in printed form via KIT Scientific Publishing.

In case of any questions please contact the workshop organizers.