

Augmenting the Curriculum targeting Hardware-aware System Design

Oliver Mattes, Fabian Nowak, Rainer Buchty, and Wolfgang Karl
Universität Karlsruhe (TH)

Institute of Computer Science & Engineering, Chair for Computer Architecture
Zirkel 2, 76131 Karlsruhe, Germany
{mattes|nowak|buchty|karl}@ira.uka.de

Abstract—In this paper we present the setup and outcome of our undergrad lab course targeting basic computer engineering and hardware design. During this course, the students get acquainted with the design process using current FPGA technology. In addition to developing own designs, the students are also required to understand provided code, adapt it for the given FPGA hardware platform, and enhance it by additional features.

I. INTRODUCTION

As part of the computer science studies at Universität Karlsruhe (TH), computer engineering is taught from the very beginning by the dedicated two-term lecture *Technische Informatik* accompanied by compulsory elective lab courses. One of these lab courses, introduced in winter term 2008, focuses on hardware design using dedicated hardware-design languages and state-of-the-art reconfigurable logic devices (FPGA). This paper presents an overview of this lab course and the experiences collected over a one-year period.

II. APPROACHES FOR TEACHING

The content of the lab is divided into up to 6 tutorials focusing on one topic which is broken down into several subtasks. A thorough introduction to each of the tasks takes place prior to working on these exercises, introducing tools to be used and solution strategies. Further information has to be obtained autonomously by the students from hand-out information and autonomous literature research.

Subsequent exercises are build on top of the results of the previous exercise. Within a single exercise the tasks to be fulfilled are structured accordingly. For each exercise, a lab report needs to be written and the achieved results presented to the entire course. An additional oral examination ensures that the presented work is authentic and understood. By being required to search additional information independently, the students further learn how to properly conduct literature research and information retrieval.

III. CONTENTS OF THE LAB COURSE

When entering this course, the students typically have no prior university-taught knowledge of hardware design. Hence, this lab course is successively teaching the use of design languages, simulation environments, and hardware design using FPGA evaluation boards. By executing provided tutorials, the students get first acquainted with the basics of the hardware-description language VHDL and according simulation tools,

Modelsim [1] and ghdl [2]. In a second introductory step, the students are then required to perform FPGA-targeted design synthesis using the vendor-specific Xilinx ISE [3] toolflow.

This is followed by the implementation of simple design examples such as simple arithmetic operations targeting the used FPGA development boards [4] and using their basic input and output devices such as switches and LEDs. Then, more complicated examples teach the use of clocked designs by implementing simple counters and a basic LED running light. The latter is subsequently extended, offering several running modes and patterns selected through the board's DIP switches.

The FPGA board offers a VGA output which is used in the next lab task: here, the students are first required to generate proper VGA timing signals, later generating stable test patterns and pictures. This VGA output circuitry is the basis of subsequent work targeting dynamic interference of individual display objects, leading to a self-programmed imitation of the well-known game Pong [5]. The basic imitation is subsequently expanded by extra functions defined by the students themselves such as a computerized opponents, multi-player mode, or other enhancements of the game-play.

The lab course is completed with porting a given imitation of the original gaming-machine hardware of the game Space Invaders [6], [7]. For this, the students have to analyze provided VHDL files and rewrite specific parts to match the available FPGA board to finally getting to run the provided ROM images. This exercise is inspired by the local RetroGames e.V. [8], delivering a sustainable emulation platform for vintage gaming hardware.

IV. CONCLUSION

Through the presented lab course, the students obtain a thorough basic training in the entire hardware-design process including description, simulation, and synthesis.

As of now, the lab course took place twice – with an increasing number of participants. We found the dedication and motivation of the students for this topic to be very high as demonstrated by the outcome of the individual exercises. A significant number of the participants of this course continue their studies in the field of computer engineering, e.g. conducting their Bachelor thesis or semester project on a related topic, joining as student assistants, or enjoying this topic in their spare time as a new-found hobby, making the lab course a success for both, students and teachers.

REFERENCES

- [1] Mentor Graphics ModelSim, <http://www.model.com/>
- [2] GHDL, <http://ghdl.free.fr/>
- [3] Xilinx ISE, <http://www.xilinx.com/ise/>
- [4] Xilinx Spartan-3A DSP Board, <http://www.xilinx.com/products/devkits/HW-SD1800A-DSP-SB-UNI-G.htm>
- [5] Pong, <http://www.pong-story.com/>
- [6] Space Invaders, <http://www.spaceinvaders.de/>
- [7] FPGArcade, http://www.fpgaarcade.com/spc_main.htm
- [8] Retrogames e.V., <http://retrogames.info/>